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Fault Tolerant Nanoscale Structures and Related Delay

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Abstract

Redundancy is a method in the system for designing fault tolerant structure with the Nanoscale gate in electronic systems. Until now, many ways are represented for this purpose, which increases complexity or decreases the system's reliability. In this paper, we compare two methods for designing a fault-tolerant structure with Nanoscale gates. These ways are NAND Multiplexing (NM) and Averaging Cells (AC). The results of simulation that evaluate the area cost and reliability of the gates indicates that NM based gates are more reliable than AC gates when the error probabilities of the circuit parts are lower than 0.003. However, when this value is exceeded (which is expected for electronic nanotechnologies), AC gates are more reliable at a lower area cost. In this paper, we show comparing the NM and the AC in the aspect of the delay parameter. It indicates that the AC method has a constant delay, but the NM system's delay will rise with increasing redundancy. As a result, the AC method's overhead for designing a fault-tolerant system with the Nanoscale gate is lower than the NM method in the aspect of the area and delay time with better reliability.

Keywords: Fault-Tolerance, NAND Multiplexing, Averaging Cell, Delay, reliability.

Introduction

Due to the foreseeable limitations of the silicon-based technology and the promising results of new devices of different nature working at the nanometer level, there is worldwide attention to the research and development of modern electronic devices that could be the base of this future technology [1][2].

Two emerging nanoscale research devices are named Nanowire Field-Effect Transistors (NWFETs), and Tunnel Field-Effect Transistors (TFETs).

Nanowire Field-Effect Transistors (NWFETs) is structured to replace the conventional planar MOSFET channel with a semiconducting nanowire. In these nanodevices, current flows through the nanowire or is pinched off under the control of the voltage on the gate electrode, which surrounds the nanowire. For this reason, they are also known as "gate-all-around" transistors. However, because of their small size, single nanowires can't carry enough current to make an efficient transistor. Researchers are currently working on the gate-all-around transistor architectures based on a small forest of nanowires controlled by the same gate and acting as a single transistor [3, 4].

Tunnel Field-Effect Transistors (TFETs) are gated reverse-biased p-i-n junctions whose switching behaviors expected to be much steeper than the conventional MOSFETs that have 60 mV/Dec subthreshold swing at room temperature. Power dissipation is one of the main limitations of the future nanoelectronic circuits. Decreasing the supply voltage reduces the energy required for switching. Still, current FETs require at least 60 mV of gate voltage to increase the current by one order of magnitude at room temperature. TFETs avoid this limit by using quantum-mechanical band-to-band tunneling, rather than a thermal injection, to inject charge carriers into the device channel [3, 5].

We clarify the meaning of three different terms in computing technology, which are strictly related to the system reliability analysis, namely defect, fault, and error. A defect is a physical problem with a final manufactured system that differs from the intended design due to an imperfect fabrication process. A fault is an incorrect state of a system due to the manufacturing defects, component failures, environmental conditions, or even improper design. A fault is active when it causes an error, otherwise, it is dormant. Error is an incorrect output of a system. The cause of an error is always a fault [3].

Electronic gates exhibit a specific error rate due to several uncertainty sources cosmic. The shrinking of the electronic devices near the atomic scale, [6] increases the effect of these error sources. Therefore, as electronic technology goes into the deep Nanoscale, the device

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reliability decreases rapidly [6]. The power supply voltage scaling that reduces the maximum density of dissipated energy reduces the noise margins too. This can lead to extremely low signal-to-noise ratios (approaching 0–1 dB [7]) and increases the gate sensitivity to device parameter variation, which is currently a cause of yield reduction [8]. It is expected to become even more relevant in the near future [9]. Predictions for Nanoscale technologies indicate that the device reliability will decrease several orders of magnitude [10] so that current implementations confirm this tendency [11].

To build reliable electronic systems using electronic nanotechnologies, it is necessary to include fault and defect tolerant capabilities into the electronic systems.

In the nano CMOS circuit, faults occur at three levels, such as gate level, circuit level, and switch level. Paper [12] discusses the switch level faults of stuck-open or stuck-off and stuck-short or stuck-on that frequently occurs in CMOS switches.

The error sources have very different characteristics and ways to affect the victim gate. Therefore, the design of a reliable system will require several layers of different tolerant techniques [2]. Current tolerant mechanisms use hardware redundancy to detect and/or correct the errors. The most utilized techniques are NAND Multiplexing (NM) and majority voting gates, as proposed by von Neumann [13] in 1955. More recent methods based on Averaging Cells (AC) [14]–[16] and reconfiguration [17] have also been proposed.

In this paper, we compare two fault-tolerant architectures in two ways that can be used to build a first tolerant layer of logic Nano gates. Therefore, the best techniques for this level are NM (as indicated in the comparison presented in [18]) and AC (due to its simplicity). To compare both structures, we first define layouts for NM and AC NAND gates using molecular Nanodevices. To evaluate the reliability of the resulting gate considering the fabrication complexity [1] introduced Nanoscale oriented models able to estimate the error probabilities of each part composing the circuits according to their fabrication complexity. Using the physical dimensions of the gates obtained from the layouts and the proposed models [1] calculate the area cost and the error probability for those gates. Simulation results in [1] indicate that NM based gates are more reliable than AC gates when the error probabilities of the circuit parts are lower than 0.003. However, when this limit is exceeded (which is expected to be the case for electronic nanotechnologies), AC gates are more reliable at a much lower area cost.

Another parameter is the delay, which we calculate for NAND gates in both NM and AC methods. The area cost and the reliability analysis have been presented previously in [1]. In this paper, we show comparing the NM and the AC in the aspect of the delay parameter. Computing this parameter is important for the different levels of redundancy.

The paper is organized as follows: Section 2 and 3 describe the basic principles of both NM and AC fault-tolerant techniques in addition to the physical implementation for each method. Section 4 compares NM and AC in the aspect of delay. Finally, section 5 concludes.

NAND Multiplexing Structure (NM)

An NM gate replicates all the elements of the primary logic function. It adds two extra sets of redundant NAND gates and two interconnection randomizers to restitute the activation fraction of the signal bundles. This structure consists of a first stage performing the NAND operation and a second stage to restore the output value. Restoration is implemented with two NAND operations in series and intercalated randomizing blocks. This restoring unit can be replicated as many times as necessary to improve reliability level, although this implies an additional increase in overhead. Interconnection randomizers consist of elements that randomly connect the output lines of one layer to the following layer's input lines to distribute the errors along with the bundle. Fig. 1 shows the gate level for an NM NAND gate [1]. Parameters usually used to formulate the NAND multiplexing characteristics are: the number of redundant inputs and outputs, the ratio between the faulty input lines and the total number of lines N, the probability of a device producing a faulty output, the number of restoring stages added at the output.

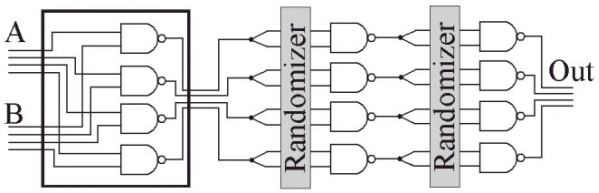

Fig.1. Scheme for a NAND Multiplexing NAND gate

Physical implementation for the NAND gates and randomizer blocks is presented in fig 2. This structure has two blocks, which the first one processes the information using a diode-like architecture, and the second one is a CMOS-like inverter that inverts the signal.

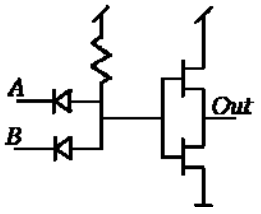

Fig.2.Circuit topology used to implement the NAND gates

A Nanodevice based layout for the NAND gate, which is drowned in [1], is presented in Fig. 3 (left). The supply voltage is connected at the top and bottom of the cell, input, and output lines on the sides. The NAND gate is consists of five devices, eleven contacts, and one interconnection. As [1] described, the NAND error probability is:

$$Perr_{NAND} = 1-(1-P_{Dev})^5 (1-\beta/(2DL+8D^2))^3(1-\beta/LD)^5(1-\beta/D^2)^3(1-(L+2D)\Upsilon/D^2) \quad (1)$$

This error probability arises from the individual error probabilities and sizes of each part of the cell. The first parenthesis corresponds to the five devices, the second, third, and fourth parenthesis to contacts 1-3, 4-8, and 9-11, respectively (see Fig. 3 left). The last parenthesis captures the error probability in the interconnection [1].

The randomizer block is built by hardwiring the outputs of one NAND stage to the inputs of the next. To analyze this block, we assume that it is possible to manufacture interconnections with sections D2 of any length.

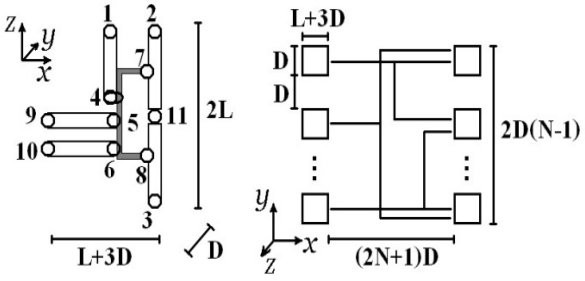

Fig.3. Proposed layout for a NAND gate (left) and a randomizer block (right) using Nanodevices.

Using the geometric information in Fig. 3 and Fig. 1, [1] estimate the area for an NM NAND gate as:

$$A_{NM} = 8N^2D^2 + 22ND^2 + 6NDL \quad (2)$$

According to Fig.1, NM structure delay is equal to eq. (3). This equation consists of a cascaded delay of three Nand gate. Each Nand gate consists of one dido and one FET transistor, according to Fig 2. Number three is the level of redundancy of the system. As a result, the final formula is equal to eq.4.

$$T_{NM}=3\ T_{diod}+ 3\ T_f \quad (3)$$

$$T_{NM}=R^*\ T_{diod}+ R^*\ T_{fet} \quad (4)$$

Averaging Cell Structure

Structure for the averaging cell gate is that it only replicates the devices (Fig. 4). The layout structure requires a significant connection able to interconnect all the Nanodevices.

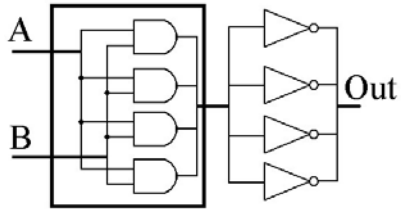

Fig.4. Scheme of a tolerant NAND gate using the averaging cell technique

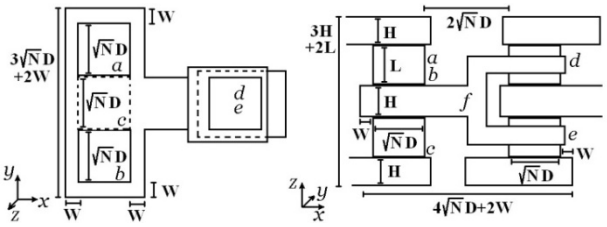

Fig.5. Proposed layout for the averaging cell NAND gate using Nanodevice clusters and metallic interconnections

From Fig. 5 we can observe that the contact areas for any given Nanodevice considerably increase with the redundancy factor (*N*). The error probability for one individual AND gate (considering that all the parts must be functional) is given by the error probability of the three devices and the six contacts that compose the gate and equivalently for the NOT gate.

$$Perr_{AND} = 1-(1-P_{Dev})^3 (1-\beta/ND^2)^6 \quad (5)$$

$$Perr_{NOR} = 1-(1-P_{Dev})^2 (1-\beta/ND^2)^4 \quad (6)$$

This structure provides a high tolerance for errors in the Nanodevices. However, errors appearing in the interconnection between the two logic functions or defects short-circuiting any Nanocluster are critical.
Then, the probability of a critical defect in the structure is approximated in [1] as:

$$Perr_{Crit} = 1-(1-ND^2{}_K)^5 (1-\beta/L\sqrt{ND})^2(1-(8\sqrt{ND})\Upsilon/ND^2) \quad (7)$$

Using the dimensions in Fig. 5, [1] estimate the area cost of this gate as:

$$A_{AC} = (3\sqrt{ND}+2W)(4\sqrt{ND}+2W) = 30ND^2 \quad (8)$$

Which has a linear dependence on the redundancy factor *N*.

According to Fig.4, the AC structure has two parts, diodes part and FETs. As a result, the delay of the AC structure is equal to eq.9.

$$T_{AC}= T_{diod}+ T_{fet} \quad (9)$$

This rate is constant and does not have any dependent on the redundancy.

Paper [19] presents a method enabling the evaluation of the averaging fault-tolerant technique, using the output probability density functions of unreliable units acquired from Monte Carlo simulations.

The heterogeneous-aware design combines averaging cells with threshold logic gates resulting in what is called Averaging Cells Linear Threshold Gates.

The key idea behind this structure was the composition of a weighted average and a threshold operation that met the main purposes of both compounding structures, namely reliable computing and implementation of Boolean functions.

Comparison of NM and AC

A comparison of NM and AC structure is possible in three aspects of area cost, reliability, and time delay. The cost and the area are critical parameters that are compared in [1]. According to eq.8 and eq.2, Fig6 present Nand gate area comparison between NM and AC structure. This comparison shows that NM is better than AC in area Cost with increasing parameter N.

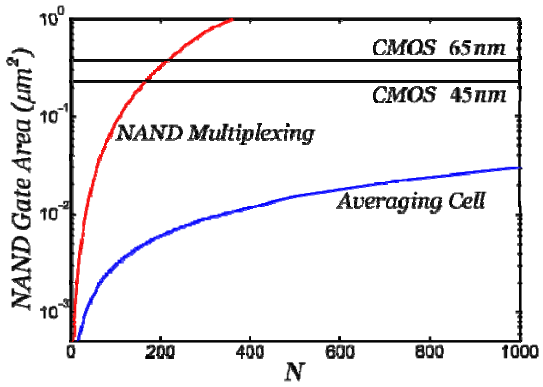

Fig.6. Area cost as the redundancy factor increases for both techniques. Constant lines indicate an estimation for a NAND gate in CMOS 65 nm and 45 nm technologies [1]

The second parameter for comparison of NM and AC structure is error probability.

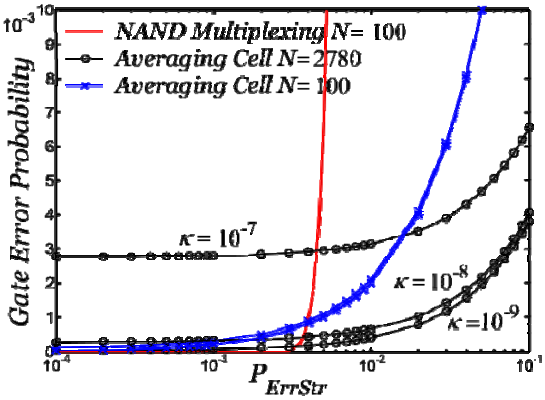

Fig.7. Error probability for a NAND gate using NAND Multiplexing technique with N =100 and using averaging cell technique with the same redundancy factor and the same area cost (N =2780) [1]

Paper [1] calculated the error probability for both structures NM and AC. Fig.7 compares the reliability of an NM NAND gate with a redundancy factor N = 100. Simulations in [1] indicate that for P_{ErrStr} below 0.003 NM provides better fault tolerant capacity. However, when the structural elements' error probability grows above this value, the gate with the AC structure presents better reliability with a lower area cost. Another factor that impacts the reliability of gates is the redundancy factor. The simulation results in [20] show that the increased probability of error in nanoscale devices may cause serious constraints on the reliability of emerging nanoelectronic circuits, as well as their fault-tolerant counterparts. In general, increasing the redundancy factor increases gate reliability.

In this paper, we compare NM and AC methods in the aspect of delay overhead, which is the third parameter for comparison. According to eq.4 and eq.9 which is calculated according to hardware structure of NM and AC, with increasing redundancy, delay of NM structure will increase, and the AC structure's delay becomes constant. We simulated and drew the time delay of two methods vs. redundancy according to eq.4 and eq.9 in the Matlab7.1 tool. Fig.8 shows this comparison in which redundancy is between 1 to 10 in horizontal axis vs. time delay in the vertical axis. Delay of diode and delay of FET transistor is preferred 5 ns. According to the delay comparison, the AC structure produces lower delay and time overhead.

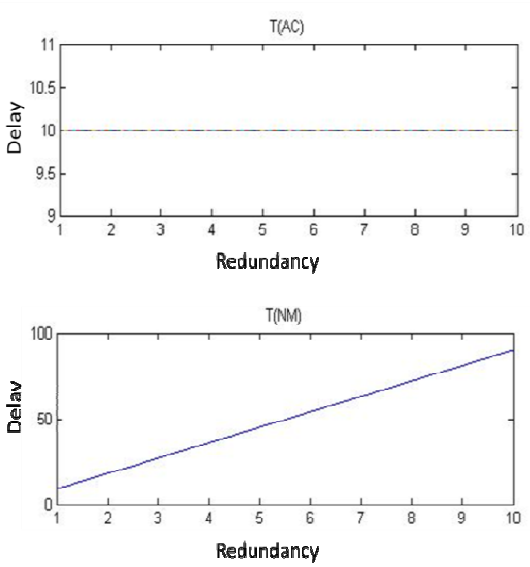

Fig.8. Time delay in NM and AC structure

NM structure has better reliability for P_{ErrStr} below 0.003 with always larger area cost and time delay, in comparison to AC structure. Therefore, If we have a system in which its P_{ErrStr} is below 0.003, we must use NM structure But if the system has P_{ErrStr} above 0.003, using AC structure will produce a more reliable system with less overhead for time delay and area cost.

By considering all three parameters of area, reliability, and delay, we can conclude that the AC structure has lower area cost, lower time delay and better reliability in most of the time for designing a fault-tolerant system in the Nanoscale gate. However, NM structure has better reliability for P_{ErrStr} below 0.003 with always larger area cost and time delay in comparison to AC structure.

Conclusion

Redundancy is necessary for the system to designing fault-tolerant structures for the Nanoscale gate in electronic systems. Until now, many methods have been proposed for this purpose, which increases complexity or has an effect on the reliability of the system. In this paper, we compare two methods for designing the fault tolerant structure for Nanoscale gates. These structures are NAND Multiplexing (NM) and Averaging Cells (AC). Simulation results in [1] indicate that AC based gates are more reliable than NM gates for higher error probabilities with lower area cost. Comparing NM and AC in the aspect of delay parameters indicates that AC has a constant delay. Still, the delay of the NM system raises with an increasing level of redundancy. We can conclude that in most cases, the AC structure has lower overhead in delay and area with higher reliability than the NM method for a fault-tolerant system.

References

[1] F. Martorell, S. D. Cotofana, and A. Rubio, "Fault tolerant structures for nanoscale gates," in 2007 7th IEEE Conference on Nanotechnology (IEEE NANO), 2007, pp. 605-610: IEEE

[2] S. D. Cotofana, A. Schmid, Y. Leblebici, A. Ionescu, O. Soffke, P. Zipf, M. Glesner, and A. Rubio, "CONAN - a design exploration framework for reliable nano-electronics architectures," in *Proceedings of 16th International Conference on Application-Specific Systems, Architectures and Processors*, July 2005, pp. 260–267.

[3] Aymerich, Nivard, et al. Variability-aware Architectures based on Hardware Redundancy for Nanoscale Reliable Computation. Diss. PhD Thesis. University Polytechnic Catalunya, 2013. xvii, 10, 2013.

[4] Katsuhiro Tomioka, Masatoshi Yoshimura, and Takashi Fukui. A iii-v nanowirechannel on silicon for high-performance vertical transistors.Nature, 488(7410):189–192, 2012.

[5] Adrian M Ionescu and Heike Riel. Tunnel field-effect transistors as energy-efficient electronic switches.Nature, 479(7373):329–337, 2011

[6] "International technology roadmap for semiconductors, ITRS," 2005. [Online]: http://www.itrs.net/Common/ 2005ITRS/ Home2005.htm

[7] H. Ahmed, "Single electron electronics: challenge for nanofabrication," *Jour. Vac. Sci & Tech. B*, vol. 15, pp. 2101–2108, 1997.

[8] R. Rao, A. Devgan, D. Blaauw, and D. Sylvester, "Analytical yield prediction considering leakage/performance correlation," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 25, pp. 1685–1695, 2006.

[9] X. Tang, V. K. De, and J. D. Meindl, "Intrinsic MOSFET parameter fluctuations due to random dopant placement," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 5, no. 4, pp. 369– 376, 1997.

[10] A. Kleinosowski, V. Pai, V. Rangarajan, P. Ranganath, K. Kleinosowski, M. Subramony, and D. Lilja, "Exploring fine-grained fault tolerance for nanotechnology devices with the recursive nanobox processor grid," *IEEE Transactions on Nanotechnology*, vol. 5, pp. 575–586, 2006.

[11] J. E. Green, J. W. Choi, A. Boukai, Y. Bunimovich, E. JohnstonHalperin, E. DeIonno, Y. Luo, B. A. Sheriff, K. Xu1, Y. S. Shin, H.R. Tseng, J. F. Stoddart, , and J. R. Heath, "A 160-kilobit molecular electronic memory patterned at 10^{11} bits per square centimetre," *Nature*, vol. 445, pp. 414–417, Jan. 2007.

[12] D. Manimekalai and P. Dixit, "Analysis of reliability for fault tolerant design in NANO CMOS logic circuit," International Journal of Nanoelectronics & Materials, vol. 10, no. 2, 2017.

[13] J. von Neumann, "Probabilistic logics and the synthesis of reliable organisms from unreliable components," in *Automata Studies*, C. Shannon and J. McCarthy, Eds. Princeton University Press, Princeton N.J., 1955, pp. 43–98.

[14] A. Schmid and Y. Leblebici, "Robust circuit and system design methodologies for nanometer-scale devices and single-electron transistors," *IEEE Transactions on VLSI Systems*, vol. 12, pp. 1156–1166, 2004.

[15] F. Martorell, A. Rubio, and S. Cotofana, "Analysis of the noise and parameter variations-tolerance of the averaging cell," *Digest of Int. Workshop on Design and Test of Defect-Tolerant Nanoscale Architectures*, pp. 3.17–3.22, 2005.

[16] F. Martorell and A. Rubio, "Cell architecture for nanoelectronic design," *Proc. European NanoSystems 2006*, pp. 114–119, 2006.

[17] K. Patel and I. Markov, "Error-correction and crosstalk avoidance in DSM busses," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 12, pp. 1076–1080, 2004.

[18] K. Nikolic, A. Sadek, and M. Forshaw, "Fault-tolerant techniques for nanocomputers," *Nanotechnology*, vol. 13, pp. 357–362, 2002.

[19] M. Stanisavljevic, A. Schmid, and Y. Leblebici, "Optimization of the averaging reliability technique using low redundancy factors for nanoscale technologies," IEEE Transactions on Nanotechnology, vol. 8, no. 3, pp. 379-390, 2008.

[20] J. Han, E. R. Boykin, H. Chen, J. Liang, and J. A. Fortes, "On the reliability of computational structures using majority logic," IEEE Transactions on Nanotechnology, vol. 10, no. 5, pp. 1099-1112, 2011.